L Number	Hits	Search Text	DB	Time stamp
1	333	cobalt adj silicide same polysilicon same titanium	USPAT; US-PGPUB	2002/08/08 10:50
2	329	(cobalt adj silicide same polysilicon same titanium) and @ad<=20020123	USPAT; US-PGPUB	2002/08/08 10:03
3	874	cobalt adj silicide and polysilicon and titanium	USPAT; US-PGPUB	2002/08/08 10:50
4	180	(cobalt adj silicide and polysilicon and titanium) not (titanium adj silicide)	USPAT; US-PGPUB	2002/08/08 10:50
5	61	((cobalt adj silicide and polysilicon and titanium) not (titanium adj silicide)) and 438/533,583,586,649,655,664,682,683.ccls.	USPAT; US-PGPUB	2002/08/08 10:53
7	13	((cobalt adj silicide and polysilicon and titanium) not (titanium adj silicide)) and 257/754,755,757,768,769.ccls.	USPAT; US-PGPUB	2002/08/08 10:56
11	9	titanium same (ionized adj physical adj vapor adj deposition)	USPAT; US-PGPUB	2002/08/08 10:58

L Number	Hits	Search Text	DB	Time stamp
1	419	cobalt adj silicide same polysilicon and titanium	USPAT; US-PGPUB	2002/08/07 16:00
5	53	ionized adj physical adj vapor	USPAT; US-PGPUB	2002/08/07 15:53
6	29	(ionized adj physical adj vapor) and titanium	USPAT; US-PGPUB	2002/08/07 15:53
7	29	((ionized adj physical adj vapor) and titanium) and @ad<=20020123	USPAT; US-PGPUB	2002/08/07 16:01
10	415	(cobalt adj silicide same polysilicon and titanium) and @ad<=20020123	USPAT; US-PGPUB	2002/08/07 16:01
11	263	((cobalt adj silicide same polysilicon and titanium) and @ad<=20020123) and dielectric	USPAT; US-PGPUB	2002/08/07 16:01
13	188	(((cobalt adj silicide same polysilicon and titanium) and @ad<=20020123) and dielectric) and (opening or trench or recess or hole)	USPAT; US-PGPUB	2002/08/07 16:02

US-PAT-NO: 6410427

DOCUMENT-IDENTIFIER: US 6410427 B1

TITLE: Metal silicidation methods and methods for using same

---------- KWIC ---------

With reference to FIGS. 3A-3D, a silicidation process which efficiently
incorporates nitrogen into the formed **cobalt silicide** in a titanium/cobalt
silicidation and reversal process to reduce spiking during the silicidation
process is described. The silicidation process includes forming a **titanium**
layer 42 and then a cobalt layer 44 over a surface of a substrate assembly 40
(FIG. 3A), which by definition includes a semiconductor substrate. In the
silicidation process described with reference to FIGS. 3A-3D, the surface upon
which cobalt layer 44 is deposited is a **titanium** surface. The **titanium** is
therefore formed on a surface of a silicon region (i.e., a doped or undoped
silicon region for silicidation and metalization thereof), a **polysilicon** region
(i.e., a doped or undoped **polysilicon** region such as for formation of a
polycide line), or various other surfaces such as for interconnect between at
least two elements of a device structure such as with a polycide line (i.e.,
drain to a bit line of a device) and can be considered part of the substrate
assembly upon which the cobalt layer 44 is formed.

A layer of cobalt 121 is then formed on the **polysilicon** layer 126 in a manner
as described previously with reference to FIGS. 1A-1C. Further as described

previously, a **titanium** film cap 123 is formed over the cobalt layer 121. Upon the silicidation anneal, cobalt 121 reacts with the **polysilicon** layer 126 resulting in the **cobalt silicide** layer 128 formed over the **polysilicon** layer 126 (FIG. 5C). Thereafter, a resist 130 is utilized for patterning the polycide line 132. With the resist 130 removed, polycide line 132 is completed via wet and/or dry etching of portions of the **polysilicon** 126 and **cobalt silicide** 128 layers. The resulting polycide line, including **polysilicon** region 136 and **cobalt silicide** region 134, is shown in FIG. 5D. The formation of gate region 138 and doping of regions 140 and 142 may then be performed in accordance with conventional processing as well as other processes for completing the device desired.

US-PAT-NO: 6392302

DOCUMENT-IDENTIFIER: US 6392302 B1

TITLE: Polycide structure and method for forming polycide structure

---------- KWIC ---------

Referring now to FIG. 4, a 75-750 .ANG. thick layer 26 of cobalt is then deposited using a physical vapor deposition (PVD) technique, preferably sputtering. A thin (approximately 100 .ANG.) layer 28 of **titanium** is also deposited. The **titanium** layer is optional. The wafer 10 is then annealed at approximately 600.degree. C. for approximately 30 seconds in a nitrogen environment to cause the upper **polysilicon** layer 18 to become transformed into a **cobalt silicide** layer 30, as shown in FIG. 5. The amount of silicon consumed during the formation of the **cobalt silicide** layer 30 is approximately 3.6 times greater than the amount of cobalt. If metals other than cobalt are used, the thicknesses of the upper **polysilicon** layer 18 and the thick layer 26 will have to be adjusted accordingly. For example, the amount of nickel consumed during the formation of nickel silicide is approximately equal to (rather than 3.6 times greater than) the amount of silicon. The remaining unreacted cobalt and **titanium** are then removed. The **titanium** may be removed with an APM (amonia+hydrogen peroxide solution+pure water) solution for five minutes at 65.degree. C. The cobalt may be removed with an HPM (hydrochloric acid+hydrogen peroxide solution+pure water) solution for 30 seconds at

30.degree. C.

US-PAT-NO: 6136705

DOCUMENT-IDENTIFIER: US 6136705 A

TITLE: Self-aligned dual thickness cobalt silicide layer formation process

---------- KWIC ---------

A process for the controlled formation of self-aligned dual thickness **cobalt silicide** layers during the manufacturing of a semiconductor device that requires a minimum number of steps and is compatible with standard MOS processing techniques. In the process according to the present invention, a semiconductor device structure (such as an MOS transistor) is first provided. The semiconductor device structure includes exposed silicon substrate surfaces (such as shallow drain and source regions) and a silicon layer structure disposed above the semiconductor substrate surface (such as a **polysilicon** gate). A cobalt layer is then deposited over the semiconductor device structure followed by the deposition of a **titanium** capping layer. Next, the thickness of the **titanium** capping layer above the silicon layer structure (e.g. a **polysilicon** gate) is selectively reduced using, for example, chemical mechanical polishing techniques. Cobalt from the cobalt layer is subsequently reacted with silicon from the exposed silicon substrate surfaces to form a first self-aligned **cobalt silicide** layer on these surfaces. At the same time, cobalt from the cobalt layer is reacted with silicon from the silicon layer structure to form a second self-aligned **cobalt silicide** layer thereon, which is

thicker than the first self-aligned **cobalt silicide** layer.

In the process according to the present invention, a semiconductor device structure (such as an MOS transistor) is first provided. The semiconductor device structure includes a silicon substrate with at least one exposed silicon substrate surface (such as a source or drain region of an MOS transistor), as well as a silicon layer structure with an exposed silicon surface disposed above the semiconductor substrate surface (such as a **polysilicon** gate of an MOS transistor). A cobalt layer is then deposited over the semiconductor device structure, followed by a deposition of a **titanium** capping layer on the cobalt layer. The thickness of the **titanium** capping layer above the silicon layer structure (e.g. a **polysilicon** gate) is thereupon selectively reduced using, for example, chemical mechanical polishing techniques. The thickness reduction process employed here is referred to as "selective" since it preferentially reduces the **titanium** capping layer thickness in one area, such as above the silicon layer structure, over that in other areas, such as above the exposed silicon substrate surface. Cobalt in the cobalt layer is then reacted with silicon in the exposed silicon substrate surface (e.g. source and drain regions) and the silicon layer structure (e.g. a **polysilicon** gate), thereby forming a first self-aligned **cobalt silicide** layer on the exposed silicon substrate surface and a second self-aligned **cobalt silicide** layer on the silicon layer structure. The second self-aligned **cobalt silicide** layer on the silicon layer structure is thicker than the thickness of the first self-aligned **cobalt silicide** layer on the exposed silicon substrate surface.

The motivation for selectively reducing the thickness of the **titanium** capping layer above the **polysilicon** gate is based on the discovery that the thickness of **cobalt silicide** layers resulting from a reaction of cobalt in the cobalt layer with the directly underlying silicon is inversely related to the thickness of the **titanium** capping layer overlying the very cobalt layer. Table 1 below lists the sheet resistance data of **cobalt silicide** layers formed underneath of a **titanium** capping layer of various thicknesses, namely a 150 angstrom **titanium** (Ti) capping layer, a 75 angstrom Ti capping layer and a **titanium** nitride (TiN) capping layer in the absence of a Ti capping layer. All other factors were held constant in obtaining these data. The data in Table 1 demonstrate that the **cobalt silicide** layer thickness, which is inversely proportional to sheet resistance of the **cobalt silicide** layer itself, is a function of **titanium** capping layer thickness.

It is believed that the "prevention effect" of the **titanium** capping layer on the formation of a **cobalt silicide** layer plateaus for **titanium** capping layers above 150 angstroms in thickness. Processes according to the present invention, however, can controllably form self-aligned dual thickness **cobalt silicide** layers by selectively reducing the **titanium** capping layer thickness over those areas where a thicker **cobalt silicide** layer is desired, while maintaining the **titanium** capping layer thickness substantially unaffected by the selective reduction process over the other areas where a thinner **cobalt silicide** layer is desired. For example, a thicker **cobalt silicide** layer may be desired over the **polysilicon** gate for increasing its conductivity, while a

thinner cobalt silicon layer may be desired over the shallow drain and source regions for preventing junction spiking.

When the "complete" reduction of the **titanium** capping layer occurs, either purposely or inadvertently, during the selective reduction step, a minimal reduction in thickness of the cobalt layer disposed directly above the **polysilicon** gate is permissible. However, since the purpose of the process according to the present invention is to produce a relatively thick **cobalt silicide** layer on the **polysilicon** gate, a significant reduction in thickness of the cobalt layer disposed directly above the **polysilicon** gate would be counterproductive.

Since the height of the **polysilicon** gate above the semiconductor substrate is the controlling factor in providing a selective reduction in thickness of the **titanium** capping layer disposed above the **polysilicon** gate during CMP processing, processes according to the present invention can be used to form a relatively thick **cobalt silicide** layer on any silicon layer structure that is taller than (i.e. higher or disposed above) the exposed silicon substrate surface on which a formation of a relatively thin **cobalt silicide** layer is desired.

Following the step of reducing the **titanium** capping layer thickness above the **polysilicon** gate, cobalt in the cobalt layer 118 that is in direct contact with silicon in the shallow drain region 106, shallow source region 108, and **polysilicon** gate 110 is reacted to form self-aligned dual thickness **cobalt silicide** (CoSi) layers 122, 124 and 126 on these regions (see FIG. 8). Since

the thickness of the **titanium** capping layer 120 above the **polysilicon** gate 110 was selectively reduced relative to its thickness above the shallow drain and source regions 106 and 108, the resultant **cobalt silicide** (CoSi) layer 126 above the **polysilicon** gate 110 is thicker than **cobalt silicide** (CoSi) layers 122 and 124 that are formed above the shallow drain and source regions 106 and 108, respectively. By manipulating the relative thicknesses of the **titanium** capping layer above the **polysilicon** gate versus above the shallow drain and source regions, self-aligned dual thickness **cobalt silicide** layers can be formed in a controllable manner.

The term "self-aligned" used in connection with the present invention serves as a dual reference: one is that the **cobalt silicide** layers 122, 124 and 126 are "self-aligned" to the silicon surfaces of the shallow drain region 106, shallow source region 108, and **polysilicon** gate 110, respectively; and the other is that a relatively thick **cobalt silicide** layer 126 is "self-aligned" to the **polysilicon** gate 110, while relatively thin **cobalt silicide** layers 122 and 124 are "self-aligned" to the shallow drain and source regions 106 and 108. This "self-aligned" nature of the dual thickness **cobalt silicide** layers is a result of the implementation of the selective reduction step of the **titanium** capping layer thickness above the **polysilicon** gate 110.

Next, the cobalt layer 118 (i.e. unreacted cobalt from the cobalt-silicon reaction to form a **cobalt silicide** layer) and the **titanium** capping layer 120 are removed using a conventional selective wet etch, such as a mixture of sulfuric acid and hydrogen peroxide, or a mixture of phosphoric acid, acetic

acid, nitric acid and hydrogen peroxide. The resultant structure, illustrated in FIG. 9, includes a relatively thin self-aligned **cobalt silicide** (CoSi) layers 122 and 124 on the shallow drain region 106 and the shallow source region 108, respectively, and a relatively thick self-aligned cobalt salicide layer 126 on the **polysilicon** gate 110. A second thermal step is then used to convert the **cobalt silicide** (CoSi) layers to **cobalt silicide** (CoSi.sub.2) layers. This second thermal can be conducted in an RTP at 650-850.degree. C. for 30 seconds to 2 minutes in an N.sub.2 ambient.

layer 128 is deposited over the **titanium** capping layer, as illustrated in FIG. 10. The **titanium** capping layer 120 is capable of gettering oxygen during the silicide formation process, and thus preventing undesirable cobalt layer oxidation, by isolating the cobalt layer from oxygen that may be in the processing environment. This appears to be true even if the **titanium** capping layer has been completely removed during the selective reduction step from above the **polysilicon** gate 110, since the **titanium** capping layers above the shallow drain and source regions 106 and 108 provide a sufficient "oxygen gettering" mechanism for the entire MOS transistor structure. The presence of a TiN capping layer 128 provides additional assurance by further isolating the cobalt layer from oxygen that may be in the processing environment. The TiN capping layer is not known to have any adverse interactions with cobalt as far as the formation of **cobalt silicide** layers is concerned. The TiN capping layer can be deposited by sputtering or CVD and has a typical thickness of around 200 angstroms.

Next, as described above with respect to the embodiment

illustrated in FIGS. 4-9, cobalt in the cobalt layer 118 that is in direct contact with silicon in the shallow drain region 106, the shallow source region 108, and the **polysilicon** gate 110 is reacted to form self-aligned dual thickness **cobalt silicide** (CoSi) layers 122, 124 and 126 on these regions (see FIG. 11). The cobalt layer 118 (i.e. unreacted cobalt from the cobalt-silicon reaction to form a **cobalt silicide** layer), the **titanium** capping layer 120 and the TiN capping layer 128 are then removed using a conventional selective wet etch, such as a mixture of sulfuric acid and hydrogen peroxide, or a mixture of phosphoric acid, acetic acid, nitric acid and hydrogen peroxide. The resultant structure, equivalent to that illustrated in FIG. 9, includes a relatively thin self-aligned **cobalt silicide** (CoSi) 122 and 124 layers on the shallow drain region 106 and the shallow source region 108, respectively, and a relatively thick self-aligned **cobalt silicide** layer 126 on the **polysilicon** gate 110. A second thermal step, similar to the one described above, is subsequently performed.

US-PAT-NO: 6268284

DOCUMENT-IDENTIFIER: US 6268284 B1

TITLE: In situ titanium aluminide deposit in high aspect ratio features

---------- KWIC ---------

A method to deposit a composite metal to form a continuous, smooth film in high aspect ratio features such as vias, contacts and/or trenches on a wafer in a single step. Metal atoms are sputtered from a composite target containing a first metal and a second metal in a single reaction chamber. A physical vapor deposition processes such as **ionized physical vapor deposition** (IPVD) is preferred. In one embodiment, the first metal is **titanium** and the second metal is aluminum. The method eliminates a high temperature anneal and results in lower resistivity, a better wetting layer for subsequent deposition and improved control over thickness of the metal layer.

The invention is also directed to a method of forming a contact plug in a via comprising depositing a first layer comprising a first metal and a second metal deposited simultaneously from a composite target of the first metal and second metal in a single reaction chamber, and then depositing a second layer of a metal to fill the via. The first metal may be either **titanium** or tungsten and the second metal may be aluminum or silicon. The first metal and second metal may be deposited by sputtering the composite source, such as by **ionized physical vapor deposition**. The method is useful for forming a contact plug in

a high aspect ratio via and can be used to deposit a film layer of different
stoichiometric quantities of the first metal and the second metal to form, for
example, a **titanium** rich bottom region of the via.

	U	1 [1]	Document ID	Issue Date	Pages
1	☐	☒	US 20020068446 A1	20020606	10
2	☐	☒	US 6410427 B1	20020625	26
3	☐	☒	US 6392302 B1	20020521	22
4	☐	☒	US 6136705 A	20001024	11
5	☐	☒	US 6103610 A	20000815	12
6	☐	☒	US 6040606 A	20000321	11

	Title	Current OR	Current XRef
1	Method of forming self-aligned silicide layer	438/664	438/299
2	Metal silicidation methods and methods for using same	438/655	438/664; 438/683; 438/902
3	Polycide structure and method for forming polycide structure	257/775	257/754; 257/767
4	Self-aligned dual thickness cobalt silicide layer formation process	438/682	438/533; 438/558; 438/584; 438/586; 438/649; 438/683
5	Integrated circuit structure with dual thickness cobalt silicide layers and method for its manufacture	438/592	438/655; 438/682
6	Integrated circuit structure with dual thickness cobalt silicide layers and method for its manufacture	257/384	257/413

	Retrieval Classif	Inventor	S	C	P	2	3	4	5
1		Wu, Yi-Ju et al.	☒	☐	☐	☐	☐	☐	☐
2		Hu, Jeff	☒	☐	☐	☐	☐	☐	☐
3		Hu, Yongjun Jeff	☒	☐	☐	☐	☐	☐	☐
4		Blair, Christopher S.	☒	☐	☐	☐	☐	☐	☐
5		Blair, Christopher S.	☒	☐	☐	☐	☐	☐	☐
6		Blair, Christopher S.	☒	☐	☐	☐	☐	☐	☐

	Image Doc. Displayed	PT
1	US 20020068446	☐
2	US 6410427	☐
3	US 6392302	☐
4	US 6136705	☐
5	US 6103610	☐
6	US 6040606	☐

DOCUMENT-IDENTIFIER: US 20020031911 A1

TITLE: Method of manufacturing a copper metal wiring in a semiconductor device

---------- KWIC ---------

[0005] A method of forming a metal wiring in a semiconductor device employs a method by which a thin **titanium** (Ti) film is deposited and then aluminum (Al) is deposited by a physical vapor deposition (hereinafter called "PVD") method or a chemical vapor deposition (hereinafter called "CVD") method, or a method by which thin tantalum (Ta) or tantalum nitride (TaN) film as a diffusion prevention film is formed by a PVD method and Cu is then deposited by an electro-plating method. The former method, however, has a problem when applied to next-generation high-performance semiconductor devices since Al has a higher resistance than Cu. On the other hand, the latter method has a limited burial characteristic of Cu due to rapid reduction in the size of the contact and increased aspect ratio. Also, as the tantalum nitride film used as a diffusion prevention film against Cu has a high resistance compared to Al to which the diffusion prevention film is not applied, there is a problem that a very thin film is required. As such, applying a copper wiring using aluminum wiring and electro-plating to next-generation semiconductor devices causes several problems.

[0015] The diffusion barrier layer 15 is formed by depositing **titanium** nitride (TiN) by means of one of an ionized PVD method, a CVD method and a MOCVD

method, depositing tantalum or tantalum nitride (TaN) by means of an ionized
PVD method or CVD method, depositing tungsten nitride (WN) by means of a CVD
method, or depositing any one of **titanium** aluminum nitride (TiAlN), **titanium**
silicon nitride (TiSiN), tantalum silicon nitride (TaSiN) by means of a PVD
method or CVD method.

[0016] Referring now to FIG. 1b, a seed layer 16 is formed on the entire
structure on which the diffusion barrier layer 15 is formed or a plasma
treatment is performed so that the chemical enhancer can be uniformly adhered.
At this time, the seed layer 16 is formed in thickness of 5 to 500 .ANG.using
one of **titanium** (Ti), aluminum (Al) and copper (Cu).

3. The method of manufacturing a copper metal wiring in a semiconductor device
according to claim 1, wherein said diffusion barrier layer is formed by
depositing **titanium** nitride (TiN) by means of one of an **ionized physical vapor**
deposition (PVD) method, a chemical vapor deposition (CVD) method and a metal
organic chemical vapor deposition (MOCVD) method, by depositing tantalum or
tantalum nitride (TaN) by means of an ionized PVD method or a CVD method, by
depositing tungsten nitride (WN) by means of a CVD method, or by depositing any
one of **titanium** aluminum nitride (TiAlN), **titanium** silicon nitride (TiSiN),
tantalum silicon nitride (TaSiN) by means of a PVD method or a CVD method.

5. The method of manufacturing a copper metal wiring in a semiconductor device
according to claim 4, wherein said seed layer is formed in thickness of between
5 and 500 .ANG. using one of **titanium** (Ti), aluminum (Al) and copper (Cu).

	U	1 [1]	Document ID	Issue Date	Pages
1	☐	☒	US 20020072181 A1	20020613	16
2	☐	☒	US 20020048878 A1	20020425	11
3	☐	☒	US 20020037624 A1	20020328	15
4	☐	☒	US 20020017670 A1	20020214	10
5	☐	☒	US 6372665 B1	20020416	10
6	☐	☒	US 6323078 B1	20011127	9
7	☐	☒	US 6316359 B1	20011113	13
8	☐	☒	US 6265262 B1	20010724	23
9	☐	☒	US 6127258 A	20001003	10
10	☐	☒	US 5998873 A	19991207	11

	Title	Current OR	Current XRef
1	Fabrication of transistor having elevated source-drain and metal silicide	438/300	257/388; 257/754; 438/629; 438/648; 438/649; 438/652; 438/757
2	Method of manufacturing capacitor in semiconductor devices	438/243	438/387; 438/709
3	Capacitor and method for fabricating semiconductor device	438/396	
4	Method of forming metal oxide metal capacitors using multi-step rapid material thermal process and a device formed thereby	257/296	257/301; 257/303; 257/306
5	Method for forming a semiconductor device	438/780	
6	Method of forming metal oxide metal capacitors using multi-step rapid thermal process and a device formed thereby	438/238	257/296; 438/210; 438/239; 438/240; 438/386; 438/396; 438/399
7	Interconnect structure in a semiconductor device and method of formation	438/678	438/629; 438/637; 438/687
8	Semiconductor device and method of fabricating the same	438/253	257/306; 257/308; 257/486; 438/238; 438/239; 438/256
9	Method for forming a semiconductor device	438/625	438/627; 438/637; 438/692; 438/703; 438/785
10	Low contact resistance and low junction leakage metal interconnect contact structure	257/766	257/753

	Retrieval Classif	Inventor	S	C	P	2	3	4	5
1		Tseng, Horng-Huei	☒	☐	☐	☐	☐	☐	☐
2		Song, Chang Rock	☒	☐	☐	☐	☐	☐	☐
3		Mori, Yoshihiro et al.	☒	☐	☐	☐	☐	☐	☐
4		Bhowmik, Siddhartha et al.	☒	☐	☐	☐	☐	☐	☐
5		Watanabe, Joy Kimi et al.	☒	☐	☐	☐	☐	☐	☐
6		Bhowmik, Siddhartha et al.	☒	☐	☐	☐	☐	☐	☐
7		Simpson, Cindy Reidsema	☒	☐	☐	☐	☐	☐	☐
8		Okuno, Yasutoshi et al.	☒	☐	☐	☐	☐	☐	☐
9		Watanabe, Joy Kimi et al.	☒	☐	☐	☐	☐	☐	☐
10		Blair, Christopher S. et al.	☒	☐	☐	☐	☐	☐	☐